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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,799	12/02/2005	Satoshi Sakai	T&A-135	3056

7590 06/23/2006

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EXAMINER	
YEVSIKOV, VICTOR V	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/519,799	SAKAI ET AL.	
	Examiner	Art Unit	
	Victor V. Yevsikov	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *18-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~FB2006~~ 12-29-04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 17, 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Ota, US 2002/0047170.

Regarding claim 1, Ota teaches a method of producing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a high dielectric constant insulating film 21 over a semiconductor substrate 1 (fig. 4);

(b) forming a conductive film 4 on the high dielectric constant insulating film (fig.7);

(c) forming an insulating film 5 on the conductive film 4 (fig. 9; § 81);

(d) selectively removing the insulating film 5 thereby forming a pattern (fig. 12, § 84);

(e) etching the conductive film 4by using the insulating film 5a having the pattern as a mask thereby forming a conductor piece (fig. 13, § 84);

(f) removing the insulating film 5 (oxide, § 84) to expose the upper surface of the conductor piece 4 in a state of leaving the high dielectric constant insulating film 21 on both ends of the conductor piece 4 over the semiconductor substrate (figs.16); and

(g) depositing a metal film on the conductor piece 4 (§ 95) and forming a reaction layer 11 at a portion of contact between the conductor piece and the metal film (reference: figs. 18 with corresponding text for all these figures).

Regarding claim 2, Ota teaches the conductive film 4 is a silicon film (§ 79) and the insulating film 5 is a silicon oxide film (§ 84);

Regarding claim 3, Ota teaches the conductive film is a silicon film (§ 79) and the reaction layer is a silicide film (§ 95);

Regarding claim 4, Ota teaches the high dielectric constant insulating film 21 is a film having a specific dielectric constant of 2.0 or more (§ 75 – 77).

Regarding claim 5, Ota teaches further comprising the step of:
(h) before the step (a), forming a trench in the semiconductor region by etching the semiconductor substrate and forming another insulating film in the trench (Fig. 3), wherein the high dielectric constant insulating film has a higher specific dielectric constant than that of another insulating film (§ 73 – 77).

Regarding claim 6, Ota teaches the high dielectric constant insulating film comprises a hafnium oxide film (§ 73).

Regarding claim 7, Ota teaches removing the high dielectric constant insulating film 21 – 23 by using the conductor piece 4 as a mask, which is a step of conducting etching under the condition where the etching selectivity of the high

dielectric constant insulating film relative to the conductor piece becomes large (fig.16; § 116);

Regarding claim 8, Ota teaches removing the high dielectric constant insulating film 21 – 23 by using the conductor piece 4 as a mask, which is a step of conducting etching under the condition where the etching selectivity of the high dielectric constant insulating film relative to the conductor piece becomes large (fig.16; § 116); and forming semiconductor regions on both sides of the conductor piece by implanting an impurity to the semiconductor substrate (fig.17; §§ 92 and 93);

Regarding claim 9, Ota teaches (h) forming another insulating film 32 (§ 90) over the semiconductor substrate including a portion on the conductor piece and then anisotropically etching another insulating film 32 thereby forming sidewall films 16 on the sidewalls of the conductor piece; and

(i) removing the high dielectric insulating film 21 - 23 by using the conductor piece and the sidewall films as masks, which is a step of conducting etching under the conditions where the etching selectivity of the high dielectric constant insulating film relative to the conductor piece and the sidewall film becomes large (figs 15 and 16).

Regarding claim 25, Ota teaches in the step (f), etching is performed under the condition where the etching selectivity of the insulating film relative to the high dielectric constant insulating film is large, thereby removing the insulating film to expose the upper surface of the conductor piece in a state of

leaving the high dielectric constant insulating film on both ends of the conductor piece over the semiconductor substrate with respect to Fig. 16.

Regarding claim 10, Ota teaches a method of producing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a first insulating film 20 (fig. 25; §120) on a first region of a semiconductor substrate having the first region and a second region;

(b) forming a second insulating film 21 – 23 having a higher dielectric constant than the first insulating film on the first insulating film and the second region;

(c) forming a conductive film 4 on the second insulating film;

(d) forming a third insulating film 5 (fig. 9) on the conductive film;

(e) selectively removing the third insulating film 5 thereby forming a pattern to each of the first and second regions (Fig. 12);

(f) etching the conductive film by using the third insulating film 5 having the pattern as a mask thereby forming a conductor piece to each of the first and second regions;

(g) removing the third insulating film 5 in a state of leaving the second insulating film on both ends of the conductor piece over the semiconductor substrate; and

(h) after the step (g), depositing a metal film on the conductor piece and forming a reaction layer 11 at a portion of contact between the conductor piece and the metal film (reference: figs 29 with corresponding texts in § 117 – 125).

Regarding claims 11 – 17 and 26, the limitations have been described earlier in rejecting claims 2 – 9 and 25.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor Yevsikov whose telephone number is (571) 272-1910. The examiner can normally be reached on Monday –Thursdays 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, examiner's supervisor, William B. Baumeister, can be reached on (571) 272-1722. The fax phone numbers for the organization where this application or processing is assigned is (703) 873-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

V. Yevsikov

Victor Yevsikov
Examiner
Art Unit 2891

June 9, 2006

Asok Kumar Sarkar

ASOK K. SARKAR
PRIMARY EXAMINER